BCA/3/CC/16

PROFESSIONAL COURSE EXAMINATION, January, 2021

(3rd Semester)

BACHELOR OF COMPUTER APPLICATIONS

Course Code: BCA/3/CC/16

(Computer Organization and Architecture) (Revised)

Full Marks : 75

Time : 3 hours

(PART : A – OBJECTIVES)

(Marks : 25)

The figures in the margin indicate full marks for the questions

SECTION – A

(Marks : 15)

I. Tick (✓) the correct answer in the brackets provided: (**1 x 10 = 10)**

1. The symbolic notation used to describe the microoperation transfers among register is called
   (a) Microoperation transfer ( )
   (b) Register transfer language ( )
   (c) High level language ( )
   (d) Interrupts ( )
2. The organization of the computer is defined by
   (a) Internal registers ( )
   (b) Timing and control structure ( )
   (c) Sets of instructions ( )
   (d) All of these ( )
3. The OPR code for the operation ADD in A+B is
   (a) 00000 ( )
   (b) 00001 ( )
   (c) 00010 ( )
   (d) 00011 ( )
4. Instruction format does not contain
   (a) Mode ( )
   (b) Operation Code ( )
   (c) Address ( )
   (d) Command ( )
5. Which one is the fastest memory among the following?

(a) Cache Memory ( )
(b) Magnetic Memory ( )
(c) Hard Disk ( )
(d) Solid State Drive ( )

6. Effective Addressing is used in
   (a) Direct Addressing Mode ( )
   (b) Indirect Address Mode ( )
   (c) Immediate Address Mode ( )
   (d) Implied Addressing Mode ( )
7. Which of the following is best suitable for stack manipulation?
   (a) Prefix Notation ( )
   (b) Infix Notation ( )
   (c) Reverse Polish Notation ( )
   (d) Polish Notation ( )
8. Which one of the following is considered as the processor register?
   (a) Data Register (DR) ( )
   (b) Address Register (AR) ( )
   (c) Accumulator (AC) ( )
   (d) Instruction Register (IR) ( )
9. The register that holds an address for the memory unit is called
   (a) DAR ( )
   (b) MAR ( )
   (c) IR ( )
   (d) PC ( )
10. The best page replacement algorithm but impossible to implement is
   (a) Optimal Page Replacement ( )
   (b) FIFO Page Replacement ( )
   (c) LRU Page Replacement ( )
   (d) LFU Page Replacement ( )

II. Indicate whether the following statements are True (T) or False (F) by putting a Tick (✓) mark in the brackets provided: **(1 x 5 = 5)**

1. Every computer has its own unique instruction set.(T / F)
2. Storage in Register Stack can be accessed using FIFO.(T / F)
3. Devices that are under the direct control of the computer are said to be connected online devices (T / F)
4. R1 <-- R2 denotes transfer of information from R1 to R2.(T / F)
5. The transformation of data from main memory to cache memory is referred to as a mapping process (T / F)

SECTION – B

(Marks : 10)

Answer the following questions: **(2 x 5 = 10)**

1. (a) Write any two things that defined the internal hardware organization of a digital computer?

   OR

   (b) Differentiate between half-adder and full-adder.
2. (a) What is a computer instruction?

   OR

   (b) Differentiate between hardwired control and micro programmed control.
3. (a) What is computer architecture?

   OR

   (b) What are the two factors on which the type of instruction depends upon?

4. (a) Write any two differences between CPU and peripheral devices.

   OR

   (b) Differentiate between online devices and peripherals.

5. (a) What do you understand by multiprogramming?

   OR

   (b) Differentiate between RAM and ROM.

(PART : B – DESCRIPTIVE)

(Marks : 50)

The figure in the margin indicate full marks for the questions

1. (a) Explain Register Transfer Language briefly. **(5)**
   (b) Explain shift micro operations. Explain any three different types of shifts. (**2 +3=5)**

   OR

   (c) What is logic micro operations? Give one example of logic micro operations.**(3+2=5)**
   (d) What is micro operations? Explain briefly the four types of micro operations. (**1+4=5)**

2. (a) Explain briefly stored program organization. **(5)**
   (b) Explain computer registers. (**5)**

   OR

   (c) Explain the design of Basic computer? (**3 + 2=5)**
   (d) Explain an instruction cycle? (**5)**

3. (a) What are the reasons in which computer use addressing modes? (**5)**
   (b) Explain Central Processing Unit (CPU) organization with suitable diagram. (**5)**

OR

(c) Explain briefly Logical and bit manipulation Instructions. **(5)**

(d) Explain the General Register Organization for seven CPU registers along with suitable diagram. **(5)**

4. (a) Explain an IO module with suitable diagram. **(5)**

(b) Explain the I/O bus and interface module with suitable diagram. **(5)**

OR

(c) Explain Direct Memory Access (DMA) with suitable diagram. **(5)**

(d) Explain source-initiated handshake with suitable diagram. **(5)**

5. (a) Explain memory hierarchy system. **(5)**

(b) Compare and contrast between static RAM and dynamic RAM. **(5)**

OR

(c) Explain the principle of cache memory. **(5)**

(d) Explain direct mapping. **(5)**

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